**IN THE SPECIFICATION:**

**Please amend page 17 as follows beginning with the paragraph starting at the bottom of page 16:**

The first and second video encoders 12 and 13 are supplied with base-band video data coming from a video source, and generates video elementary streams (will be referred to simply as "video streams" hereunder) VES0 and VES1 by compressing, by encode the video data with a predetermined encoding technique such as MPEG-2 or MPEG-4. The first and second video encoders 12 and 13 divide the generated video streams VES0 and VES1 into units, and store each of the divisional units into the data memory 19 via the data bus 11. Also, the first and second video encoders 12 and 13 generate system information on the generated video streams VES0 and VES1 and which are necessary for multiplexing the [[vide]] video streams. The video encoders 12 and 13 supply the system information and storage location information (address where recording of the unit is started, and byte length of the unit) having state therein the storage location of each unit in the data memory 19 to the CPU 16 via the data bus 11.

**Please amend the paragraph on page 17 lines 10-21 as follows:**

The first and second audio encoders 14 and 15 are supplied with the base-band audio data coming from an audio source, and generates audio elementary streams (will be referred to simply as "audio streams" hereunder) AES0 and AES1 by compressing, by encoding the audio data with a predetermined encoding technique such as MPEG-2 or MPEG-4. The first and second audio encoders 14 and 15 divide the generated audio streams AES0 and AES1 into units, and store each of the divisional units into the data memory 19 via the data bus 11. Also, the first and second audio encoders 14 and 15 generate system information on the generated audio streams AES0 and AES1 and which are necessary for multiplexing the [[vide]] video streams. The audio

encoders 14 and 15 supply the system information and storage location information (address where recording of the unit is started and byte length of the unit) having state therein the storage location of each unit in the data memory 19 to the CPU 16 via the data bus 11.

**Please amend the last full paragraph on page 21 lines 19-20 as follows:**

The instruction set is composed of an instruction group 31 and table information 32 as [[sown]] shown in FIG. 6.

**Please amend page 21 as follows beginning with the paragraph at the bottom of page 21 and ending at the top of page 22:**

In the instruction group 31, there are [[state]] more than one multiplexing instruction data 33. Each of the multiplexing instruction data 33 includes necessary indication for reading one unit from the data memory 19 and supplies it as a multiplexed stream.

**Please amend the paragraph on page 25 lines 4-17 as follows:**

As shown in FIG. 8, the data memory 19 has stored therein a unit V0 ( [[recoding]] recording start address Av0 and number of bytes Nv0) and unit V1 (recording start address Av1 and number of bytes Nv1) in the first video storage area (Sv0) 21 thereof, a unit A0 (recording start address Aa0 and number of bytes Na0) and unite A1 (recording start address Aa1 and number of bytes Na1) in the first audio storage area (Sa0) 22, a unit H0 (recording start address Ah0 and number of bytes Nh0) and unit H1 (recording start address Ah1 and number of bytes Nh1) in the first header storage area (Sh0) 23, a unit V2 ([[recoding]] recording start address

Av2 and number of bytes Nv2) and unit V3 (recording start address Av3 and number bytes Nv3) in the second video storage area (Sv3) 24 thereof, a unit A2 (recording start address Aa2 and number of bytes Na2) and unit A3 (recording start address Aa3 and number of bytes Na3) in the second audio storage area (Sa1) 25, a unit H2 (recording start address Ah2 and number of bytes Nh2) and unit H3 (recording start address Ah3 and number of bytes Nh3) in the second header storage area (Sh1) 26.